04-28-00

EL465676034

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PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Please type a plus sign (+) inside this box → [+]

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1427
First Inventor or Application Identifier	Zhiping Yin
Title	Circuitry and Gate Stacks (As Amended)
Express Mail Label No.	EL465676034US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 21] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages 5]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

*NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
9. [ ] English Translation Document (if applicable)
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
13. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. [ ] Other: ....

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09/146,842
Prior application information: Examiner B. Smith Group / Art Unit 2824

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label 021567 (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

Name			
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Name (Print/Type)	David G. Latwesen, Ph.D.	Registration No. (Attorney/Agent)	40,045
Signature		Date	4/26/00

EL465676034

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/146,842
Priority Filing Date .... September 3, 1998
Inventor .... Zhiping Yin et al.
Assignee .... Micron Technology, Inc.
Priority Group Art Unit 2824
Priority Examiner .... B. Smith
Attorney's Docket No. MI22-1427
Title: Circuitry and Gate Stacks (As Amended)

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
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Spokane, WA 99201-3828

AMENDMENTS

In the Specification

Replace the title with --Circuitry and Gate Stacks--.

At p. 1, before the "Technical Field" section, insert the following:

--RELATED PATENT DATA

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/146,842, filed September 3, 1998.--

Amended Claims

Please cancel claims 1-22.

28. (Once Amended) The [circuitry] <u>gate stack</u> of claim 27 wherein the layer comprising silicon, nitrogen and oxygen comprises $Si_xN_yO_z$:H, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33.

29. (Once Amended) The [circuitry] <u>gate stack</u> of claim 27 wherein the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

30. (Once Amended) The [circuitry] <u>gate stack</u> of claim 27 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen.

31. (Once Amended) The [circuitry] <u>gate stack</u> of claim 27 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen, and the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

REMARKS

Claims 1-22 have been canceled; and claims 28-31 are amended. Claims 23-31 are pending in the application.

Respectfully submitted,

Dated: 4/26/00

By:

David G. Latwesen, Ph.D.
Reg. No. 38,533

EL465676034

EL169835254

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

*   *   *   *   *

SEMICONDUCTOR PROCESSING METHODS, SEMICONDUCTOR CIRCUITRY, AND GATE STACKS

*   *   *   *   *

INVENTORS

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ATTORNEY'S DOCKET NO. MI22-882

SEMICONDUCTOR PROCESSING METHODS, SEMICONDUCTOR CIRCUITRY, AND GATE STACKS

TECHNICAL FIELD

The invention pertains to methods of forming and utilizing antireflective materials. The invention also pertains to semiconductor processing methods of forming stacks of materials, such as, for example, gate stacks.

BACKGROUND OF THE INVENTION

Semiconductor processing methods frequently involve patterning layers of materials to form a transistor gate structure. Fig. 1 illustrates a semiconductive wafer fragment 10 at a preliminary step of a prior art gate structure patterning process. Semiconductive wafer fragment 10 comprises a substrate 12 having a stack 14 of materials formed thereover. Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with a p-type background dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate"

refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Stack 14 comprises a gate oxide layer 16, a polysilicon layer 18, a metal silicide layer 20, an oxide layer 22, a nitride layer 24, an antireflective material layer 26, and a photoresist layer 28. Gate oxide layer 16 can comprise, for example, silicon dioxide, and forms an insulating layer between polysilicon layer 18 and substrate 12. Polysilicon layer 18 can comprise, for example, conductively doped polysilicon, and will ultimately be patterned into a first conductive portion of a transistor gate.

Silicide layer 20 comprises a metal silicide, such as, for example, tungsten silicide or titanium silicide, and will ultimately comprise a second conductive portion of a transistor gate. Prior to utilization of silicide layer 20 as a conductive portion of a transistor gate, the silicide is typically subjected to an anneal to improve crystallinity and conductivity of the silicide material of layer 20. Such anneal can comprise, for example, a temperature of from about 800°C to about 900°C for a time of about thirty minutes with a nitrogen (N_2) purge.

If silicide layer 20 is exposed to gaseous forms of oxygen during the anneal, the silicide layer can become oxidized, which can adversely effect conductivity of the layer. Accordingly, oxide layer 22 is preferably provided over silicide layer 20 prior to the anneal. Oxide layer 22 can comprise, for example, silicon dioxide. Another purpose

of having oxide layer 22 over silicide layer 20 is as an insulative layer to prevent electrical contact of silicide layer 20 with other conductive layers ultimately formed proximate silicide layer 20.

Nitride layer 24 can comprise, for example, silicon nitride, and is provided to further electrically insulate conductive layers 18 and 20 from other conductive layers which may ultimately be formed proximate layers 18 and 20. Nitride layer 24 is a thick layer (a typical thickness can be on the order of several hundred, or a few thousand Angstroms) and can create stress on underlying layers. Accordingly, another function of oxide layer 22 is to alleviate stress induced by nitride layer 24 on underlying layers 18 and 20.

Antireflective material layer 26 can comprise, for example, an organic layer that is spun over nitride layer 24. Alternatively, layer 26 can be a deposited inorganic antireflective material, such as, for example, $Si_xO_yN_z$:H, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33. In practice the layer can be substantially inorganic, with the term "substantially inorganic" indicating that the layer can contain a small amount of carbon (less than 1% by weight). Alternatively, if, for example, organic precursors are utilized, the layer can have greater than or equal to 1% carbon, by weight.

Photoresist layer 28 can comprise either a positive or a negative photoresist. Photoresist layer 28 is patterned by exposing the layer to light through a masked light source. The mask contains clear and

opaque features defining a pattern to be created in photoresist layer 28. Regions of photoresist layer 28 which are exposed to light are made either soluble or insoluble in a solvent. If the exposed regions are soluble, a positive image of the mask is produced in photoresist layer 28 and the resist is termed a positive photoresist. On the other hand, if the non-radiated regions are dissolved by the solvent, a negative image results, and the photoresist is referred to as a negative photoresist.

A difficulty that can occur when exposing photoresist layer 28 to radiation is that waves of the radiation can propagate through photoresist 28 to a layer beneath the photoresist and then be reflected back up through the photoresist to interact with other waves of the radiation which are propagating through the photoresist. The reflected waves can constructively and/or destructively interfere with the other waves to create periodic variations of light intensity within the photoresist. Such variations of light intensity can cause the photoresist to receive non-uniform doses of energy throughout its thickness. The non-uniform doses can decrease the accuracy and precision with which a masked pattern is transferred to the photoresist. Antireflective material 26 is provided to suppress waves from reflecting back into photoresist layer 28. Antireflective layer 26 comprises materials which absorb and/or attenuate radiation and which therefore reduce or eliminate reflection of the radiation.

Fig. 2 shows semiconductive wafer fragment 10 after photoresist layer 28 is patterned by exposure to light and solvent to remove portions of layer 28.

Referring to Fig. 3, a pattern from layer 28 is transferred to underlying layers 16, 18, 20, 22, 24, and 26 to form a patterned stack 30. Such transfer of a pattern from masking layer 28 can occur by a suitable etch, such as, for example, a plasma etch utilizing one or more of Cl, HBr, CF_4, CH_2F_2, He, and NF_3.

After the patterning of layers 16, 18, 20, 22, 24 and 26, layers 28 and 26 can be removed to leave a patterned gate stack comprising layers 16, 18, 20, 22, and 24.

A continuing goal in semiconductor wafer fabrication technologies is to reduce process complexity. Such reduction can comprise, for example, reducing a number of process steps, or reducing a number of layers utilized in forming a particular semiconductor structure. Accordingly, it would be desirable to develop alternative methods of forming patterned gate stacks wherein fewer steps and/or layers are utilized than those utilized in the prior art embodiment described with reference to Figs. 1-3.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a semiconductor processing method. A metal silicide layer is formed over a substrate. An antireflective material layer is chemical vapor deposited in physical contact with the metal silicide layer. A layer of photoresist is applied over the antireflective material layer and patterned photolithographically.

In another aspect, the invention encompasses a gate stack forming method. A polysilicon layer is formed over a substrate. A metal silicide layer is formed over the polysilicon layer. An antireflective material layer is deposited over the metal silicide layer. A silicon nitride layer is formed over the antireflective material layer and a layer of photoresist is formed over the silicon nitride layer. The layer of photoresist is photolithographically patterned to form a masking layer from the layer of photoresist. A pattern is transferred from the masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer to pattern the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer into a gate stack.

In yet another aspect, the invention encompasses a gate stack comprising a polysilicon layer over a semiconductive substrate. The gate stack further comprises a metal silicide layer over the polysilicon layer, and a layer comprising silicon, oxygen and nitrogen over the metal

silicide. Additionally, the gate stack comprises a silicon nitride layer over the layer comprising silicon, oxygen and nitrogen.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a preliminary processing step of a prior art process.

Fig. 2 is a view of the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 2.

Fig. 4 is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a preliminary processing step of a method of the present invention.

Fig. 5 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that of Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

An embodiment encompassed by the present invention is described with reference to Figs. 4-6. In describing the embodiment of Figs. 4-6, similar numbering to that utilized above in describing the prior art processing of Figs. 1-3 will be used, with differences indicated by the suffix "a", or by different numerals.

Referring to Fig. 4, a semiconductive wafer fragment 10a is illustrated at a preliminary processing step. Wafer fragment 10a, like the wafer fragment 10 of Figs. 1-3, comprises a substrate 12, a gate oxide layer 16, a polysilicon layer 18, and a silicide layer 20. However, in contrast to the prior art processing described above with reference to Figs. 1-3, a layer 50 comprising silicon, nitrogen, and oxygen is formed over silicide 20, and in the shown preferred embodiment is formed in physical contact with silicide layer 20. Layer 50 thus replaces the oxide layer 22 of the prior art embodiment of Figs. 1-3.

Layer 50 is preferably formed by chemical vapor deposition (CVD). Layer 50 can be formed by, for example, CVD utilizing SiH_4 and N_2O as precursors, in a reaction chamber at a temperature of about 400°C. Such deposition can be performed either with or without a plasma being present within the reaction chamber. Exemplary

conditions for depositing layer 50 include flowing SiH_4 into a plasma-enhanced CVD chamber at a rate of from about 40 standard cubic centimeters per minute (SCCM) to about 300 SCCM (preferably about 80 SCCM), N_2O at a rate of from about 80 SCCM to about 600 SCCM (preferably about 80 SCCM), He at a rate from about 1300 SCCM to about 2500 SCCM (preferably about 2200 SCCM), with a pressure within the chamber of from about 4 Torr to about 6.5 Torr, and a power to the chamber of from about 50 watts to about 200 watts (preferably about 100 watts).

The above-described exemplary conditions can further include flowing nitrogen gas (N_2) into the reaction chamber at a rate of from greater than 0 SCCM to about 300 SCCM, and preferably at a rate of about 200 SCCM, and/or flowing NH_3 into the reaction chamber at a rate of from greater than 0 SCCM to about 100 SCCM.

An exemplary composition of layer 50 is $Si_XN_yO_z$:H, wherein $x=0.5$, $y=0.37$, and $z=0.13$. The relative values of x, y, z and the hydrogen content can be adjusted to alter absorbance characteristics of the deposited material. Layer 50 preferably has a thickness of from about 250Å to about 650Å.

Layer 50 is preferably provided over silicide layer 20 before annealing layer 20. Layer 50 thus provides the above-described function of oxide layer 22 (described with reference to Figs. 1-3) of protecting

silicide layer 20 from exposure to gaseous oxygen during annealing of the silicide layer.

A silicon nitride layer 24 is formed over layer 50, and can be in physical contact with layer 50. As discussed above in the background section of this disclosure, silicon nitride layer 24 can exert stress on underlying layers. Accordingly, layer 50 can serve a function of prior art silicon dioxide layer 22 (discussed with reference to Figs. 1-3) of alleviating such stress from adversely impacting underlying conductive layers 20 and 18. Silicon nitride layer 24 can be formed over layer 50 either before or after annealing silicide layer 20.

A photoresist layer 28 is formed over silicon nitride layer 24. In contrast to the prior art embodiment discussed with reference to Figs. 1-3, there is no antireflective material layer formed between silicon nitride layer 24 and photoresist layer 28. Instead, layer 50 is preferably utilized to serve the function of an antireflective material. Specifically, nitride layer 24 is effectively transparent to radiation utilized in patterning photoresist layer 28. Accordingly, radiation which penetrates photoresist layer 28 will generally also penetrate silicon nitride layer 24 and thereafter enter layer 50. Preferably, the stoichiometry of silicon, oxygen and nitrogen of layer 50 is appropriately adjusted to cancel radiation reaching layer 50 from being reflected back into photoresist layer 28. Such adjustment of stoichiometry can be adjusted with routine experimentation utilizing methods known to persons of ordinary skill in

the art. Another way of describing the adjustment of layers 24 and 50 is that layers 24 and 50 can be tuned in thickness (by adjusting thickness of one or both of layers 24 and 50) and stoichiometry (by adjusting a stoichiometry of layer 50) such that reflection back into an overlying layer of photoresist is minimized.

Referring to Fig. 5, photoresist layer 28 is patterned to form a patterned mask over a stack 60 comprising layers 16, 18, 20, 50 and 24.

Referring to Fig. 6, a pattern from photoresist layer 28 is transferred to stack 60 (Fig. 5) to form a patterned gate stack 70 comprising layers 16, 18, 20, 50 and 24. Such transfer of a pattern from layer 28 can be accomplished by, for example, a plasma etch utilizing one or more of Cl, HBr, CF_4, CH_2F_2, He and NF_3. Photoresist layer 28 can then be removed from over gate stack 70. Subsequently, source and drain regions can be implanted adjacent the gate stack, and sidewall spacers can be provided over sidewalls of the gate stack to complete construction of a transistor gate from gate stack 70.

The method of the present invention can reduce complexity relative to the prior art gate stack forming method described above with reference to Figs. 1-3. Specifically, the method of the present invention can utilize a single layer (50) to accomplish the various functions of protecting silicide during annealing, reducing stress from an overlying silicon nitride layer, and alleviating reflections of light during photolithographic processing of an overlying photoresist layer.

Accordingly, the method of the present invention can eliminate an entire layer (antireflective layer 26 of Figs. 1-3) relative to the prior art process described with reference to Figs. 1-3. Such elimination of a layer also eliminates fabrication steps associated with forming and removing the layer. Accordingly, methods encompassed by the present invention can be more efficient semiconductor fabrication processes then prior art methods.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A semiconductor processing method comprising:

forming a metal silicide layer over a substrate;

depositing a layer comprising silicon, nitrogen and oxygen over the metal silicide layer; and

while the layer comprising silicon, nitrogen and oxygen is over the metal silicide layer, annealing the metal silicide layer.

2. The method of claim 1 wherein the layer comprising silicon, nitrogen and oxygen comprises $Si_xN_yO_z$:H, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33.

3. The method of claim 2 further comprising forming a layer of silicon nitride over the layer comprising silicon, nitrogen, oxygen and hydrogen.

4. The method of claim 2 further comprising forming a layer of silicon nitride over the layer comprising silicon, nitrogen, oxygen and hydrogen before the annealing.

5. The method of claim 1 wherein the depositing comprises chemical vapor deposition.

6. The method of claim 1 further comprising forming a layer of silicon nitride over the layer comprising silicon, nitrogen and oxygen.

7. The method of claim 1 further comprising forming a layer of silicon nitride over the layer comprising silicon, nitrogen and oxygen before the annealing.

8. A semiconductor processing method comprising:

forming a metal silicide layer over a substrate;

depositing a layer comprising silicon, nitrogen and oxygen over the metal silicide layer; and

forming a layer of silicon nitride over the layer of silicon, nitrogen and oxygen.

9. The method of claim 8 wherein the layer comprising silicon, nitrogen and oxygen comprises $Si_xN_yO_z:H$, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33.

10. The method of claim 8 wherein the depositing comprises chemical vapor deposition.

11. A semiconductor processing method comprising:

forming a metal silicide layer over a substrate;

chemical vapor depositing an antireflective material layer in physical contact with the metal silicide;

forming a layer of photoresist over the antireflective material layer; and

photolithographically patterning the layer of photoresist.

12. The method of claim 11 wherein the deposited antireflective material layer comprises silicon, nitrogen and oxygen.

13. The method of claim 11 wherein the deposited antireflective material layer comprises silicon, nitrogen, oxygen and hydrogen.

14. The method of claim 11 further comprising forming a silicon nitride layer over the deposited antireflective material layer, and wherein the layer of photoresist is formed over the silicon nitride layer.

15. A gate stack forming method, comprising:

forming a polysilicon layer over a substrate;

forming a metal silicide layer over the polysilicon layer;

depositing an antireflective material layer over the metal silicide layer;

forming a silicon nitride layer over the antireflective material layer;

forming a layer of photoresist over the silicon nitride layer;

photolithographically patterning the layer of photoresist to form a patterned masking layer from the layer of photoresist; and

transferring a pattern from the patterned masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer to pattern the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer into a gate stack.

16. The method of claim 15 further comprising, while the antireflective layer is over the metal silicide layer, annealing the metal silicide layer

17. The method of claim 15 wherein the depositing comprises chemical vapor deposition.

18. The method of claim 15 wherein the deposited antireflective material layer comprises silicon, nitrogen, oxygen and hydrogen.

19. The method of claim 15 wherein the deposited antireflective material layer comprises silicon, nitrogen and oxygen.

20. The method of claim 19 wherein the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

21. The method of claim 19 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen.

22. The method of claim 19 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen, and the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

23. Circuitry comprising:

a metal silicide layer over a semiconductive substrate; and

a substantially inorganic layer comprising silicon, nitrogen and oxygen in physical contact with the metal silicide layer.

24. The circuitry of claim 23 wherein the layer comprising silicon, nitrogen and oxygen is over the metal silicide layer, and further comprising a layer of silicon nitride over the layer comprising silicon, nitrogen and oxygen.

25. The circuitry of claim 23 wherein the layer comprising silicon, nitrogen and oxygen is over the metal silicide layer, and further comprising a layer of silicon nitride over and in physical contact with the layer comprising silicon, nitrogen and oxygen.

26. The circuitry of claim 23 wherein the layer comprising silicon, nitrogen and oxygen comprises $Si_xN_yO_z$:H, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33.

27. A gate stack, comprising:

a polysilicon layer over a semiconductive substrate;

a metal silicide layer over the polysilicon layer;

a layer comprising silicon, oxygen and nitrogen over the metal silicide; and

a silicon nitride layer over the layer comprising silicon, oxygen and nitrogen.

28. The circuitry of claim 27 wherein the layer comprising silicon, nitrogen and oxygen comprises $Si_xN_yO_z:H$, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33.

29. The circuitry of claim 27 wherein the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

30. The circuitry of claim 27 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen.

31. The circuitry of claim 27 wherein the silicon nitride layer physically contacts the layer comprising silicon, nitrogen and oxygen, and the layer comprising silicon, nitrogen and oxygen physically contacts the metal silicide layer.

ABSTRACT OF THE DISCLOSURE

In one aspect, the invention includes a semiconductor processing method comprising a) forming a metal silicide layer over a substrate; b) depositing a layer comprising silicon, nitrogen and oxygen over the metal silicide layer; and c) while the layer comprising silicon, nitrogen and oxygen is over the metal silicide layer, annealing the metal silicide layer. In another aspect, the invention includes a gate stack forming method, comprising a) forming a polysilicon layer over a substrate; b) forming a metal silicide layer over the polysilicon layer; c) depositing an antireflective material layer over the metal silicide layer; d) forming a silicon nitride layer over the antireflective material layer; e) forming a layer of photoresist over the silicon nitride layer; f) photolithographically patterning the layer of photoresist to form a patterned masking layer from the layer of photoresist; and g) transferring a pattern from the patterned masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer to pattern the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer into a gate stack. In yet other aspects, the invention encompasses circuitry and gate stacks.

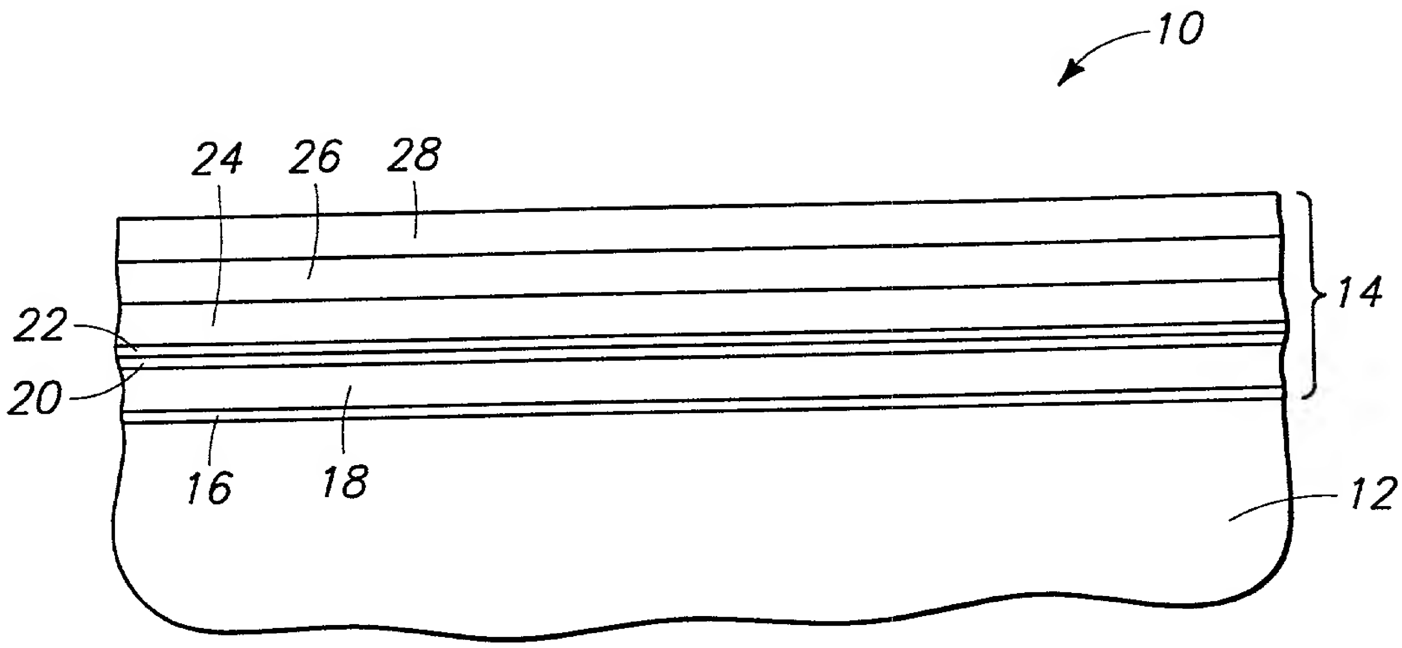

FIG 1
PRIOR ART

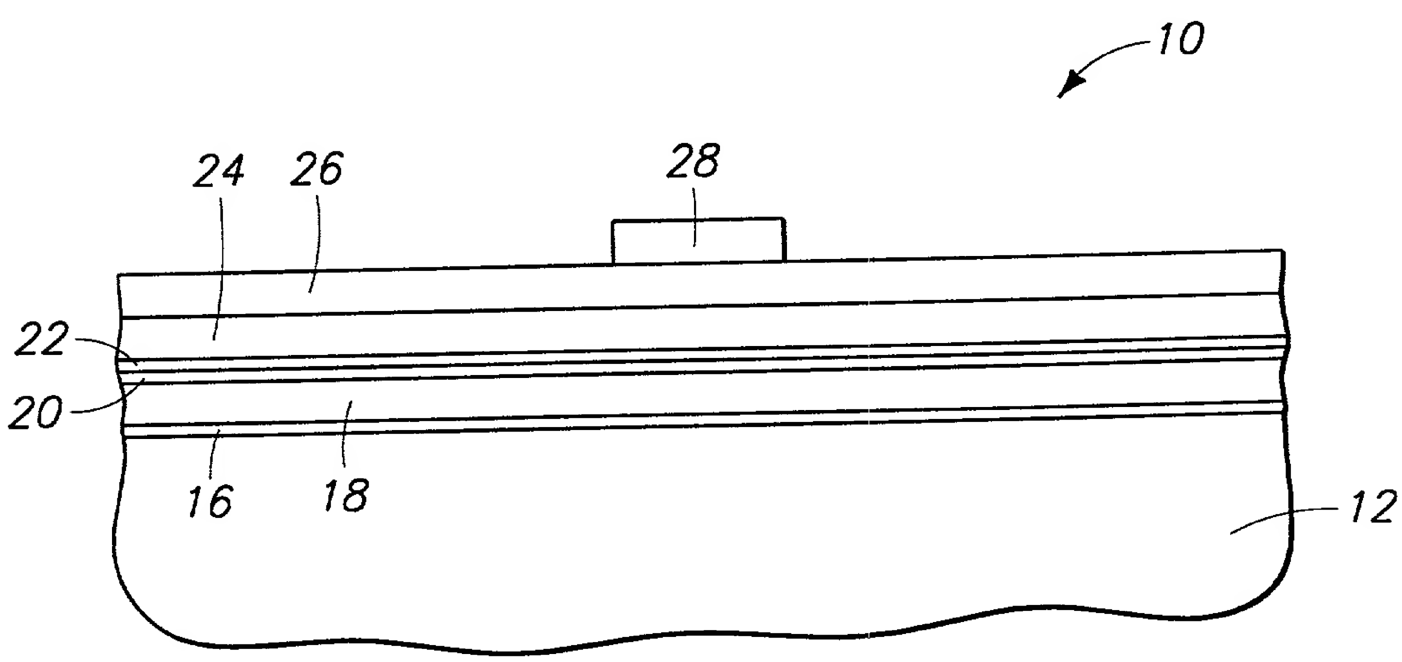

FIG 2
PRIOR ART

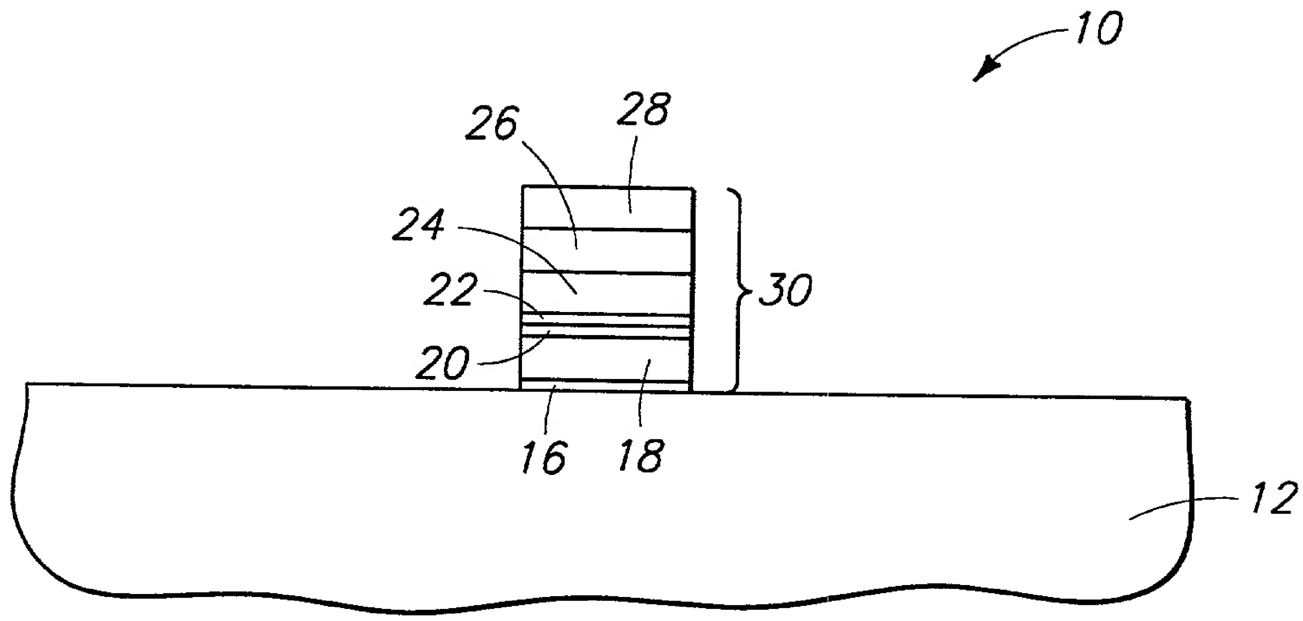

FIG 3
PRIOR ART

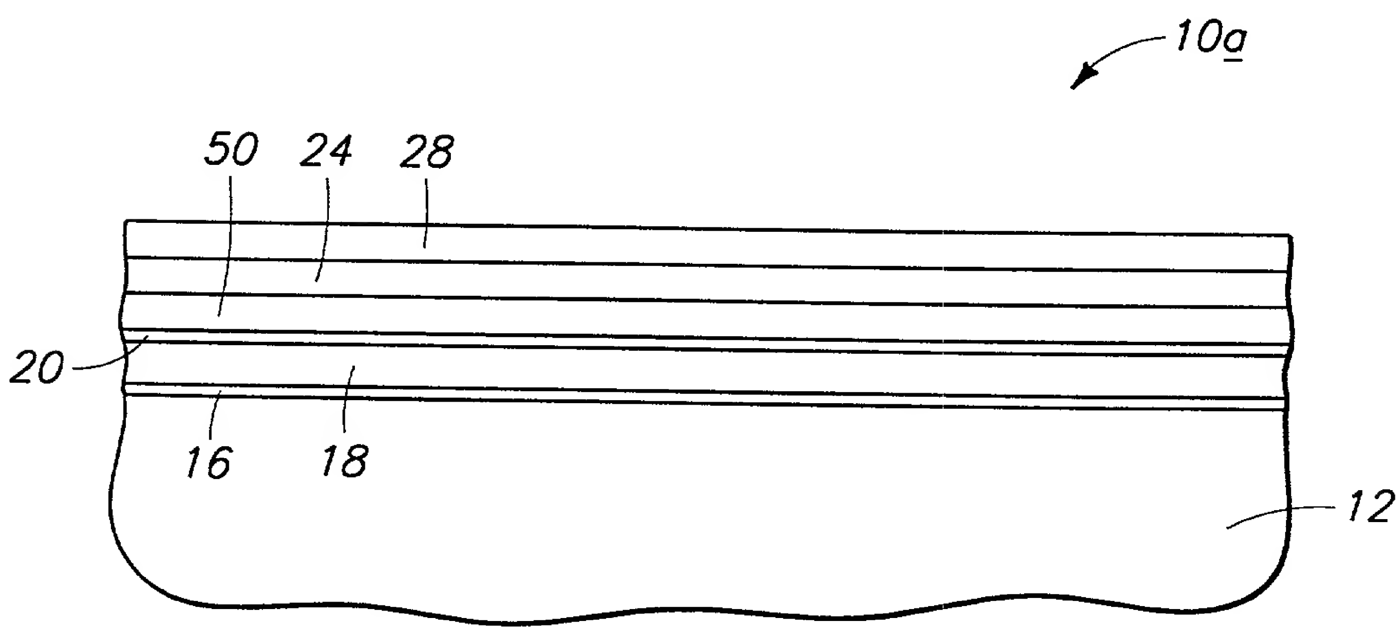

FIG 4

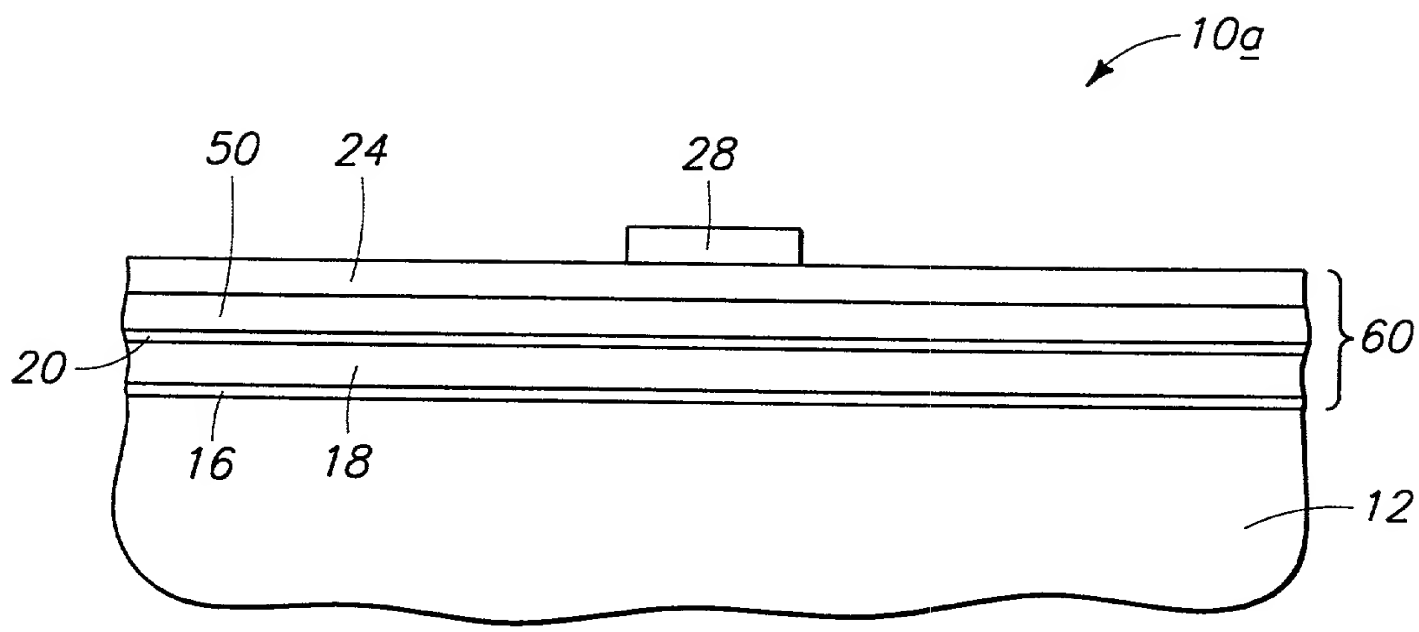

Fig 5

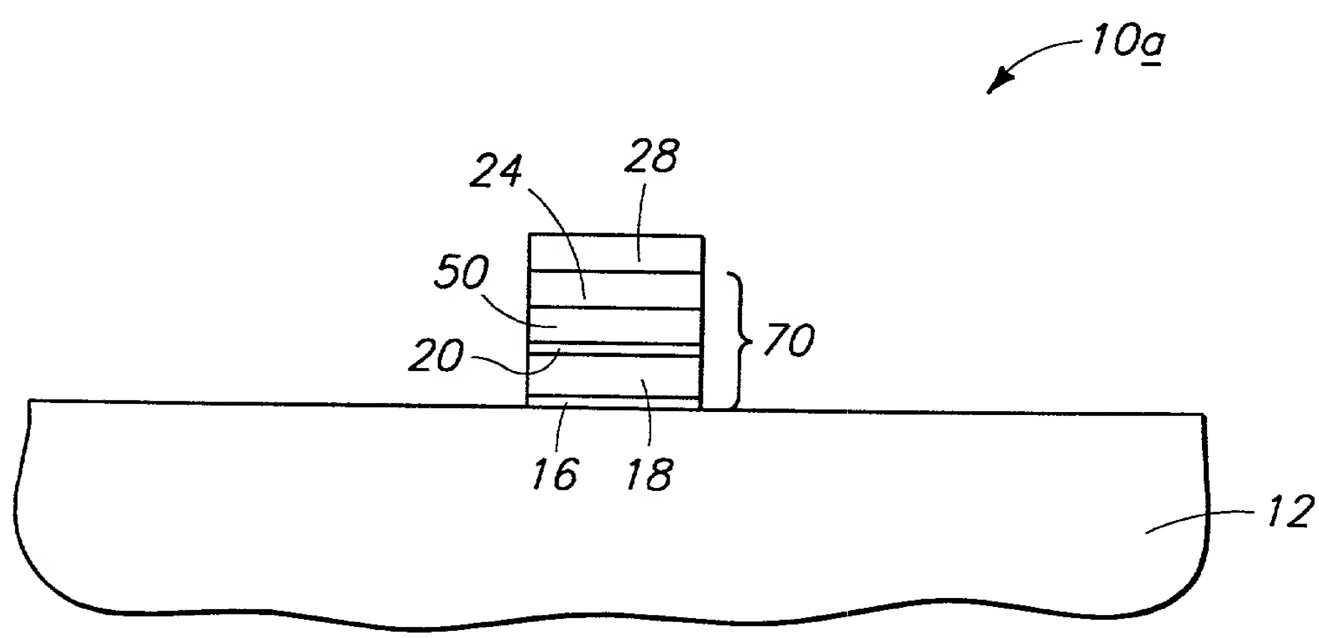

Fig 6

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Semiconductor Processing Methods, Semiconductor Circuitry, And Gate Stacks, Serial No. 09/146,842, filed September 3, 1998.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

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* * * * * * * * * *

Full name of inventor: Ravi Iyer

Inventor's Signature: Ravi Iyer

Date: 10/27/98

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